UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,249	08/18/2003	Eugene Feng	2102397-992780	4655

26379 7590 11/28/2005

DLA PIPER RUDNICK GRAY CARY US, LLP
2000 UNIVERSITY AVENUE
E. PALO ALTO, CA 94303-2248

EXAMINER	
STIGLIC, RYAN M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,249	FENG ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending and have been examined.

2. Claims 1-10 are rejected.

Response to Arguments

3. Applicant's arguments filed September 22, 2005 have been fully considered but they are not persuasive. With respect to applicant's arguments that Chang, Goetting, and Joo fail to disclose a user-selectable non-volatile memory that stores a user selected protocol, or one that generates a select signal corresponding to the user selected protocol.

In regards to Chang:

As previously stated in the Office Action dated June 22, 2005 the Examiner respectfully submits that there ***must*** be an inherent memory to hold and generate the value of EN_LPC at a logic high value because the specification of Chang supports the notion that the LPC protocol circuit (Fig. 2, 208) will be enabled to handle all future read and write operations (coil 7, ll. 43-45). Firstly figures 2 and 9 show a device collectively considered to be a memory device. The memory device stores both a LPC Protocol (Fig. 2 and 9, 208) and a FWH Protocol (Fig. 2 and 9, 206) that are user selected based on the protocol used by the host system (col. 5, ll. 64-67; "*As a result, memory device **200** may be used in motherboards having chipsets that employ either the FWH communication protocol **or** the LPC communication protocol...* "). Therefore the memory device communicates with the host system according to the user selected protocol chosen for the

host system. With regards to generating the select signal corresponding to the user-selected protocol the Examiner will further elaborate.

The memory device (Fig. 2 and 9, devices 200 and 900) is a user (programmer/system designer) defined entity that selectively chooses the operating protocol of the memory device according to the protocol, defined by the user/programmer/system designer, of the system in which it is installed. In other words if the user (of the system to which the memory device is installed) selects the LPC communication protocol for the control chipset of the system, the programmer/system designer/user of the memory device of Chang defined the memory device (Fig. 2 and 9, 200 and 900) such that the memory device selects the appropriate protocol. Therefore the communication protocol of the memory device (Fig. 2 and 9, 200 and 900) is user selectable according to the protocol employed by the system. In order to achieve this the memory device (Fig. 2 and 9, 200 and 900) initially receives a start code indicative of the protocol (col. 5, line 44 – col. 6, line 2). In response to the start code received via an operating interface (Fig. 2 and 9, 204) a protocol detection circuit (Fig. 2 and 8, devices 210 and 800) decodes the start code and outputs either a selection signal (Fig. 9, SEL) or two enable signals (Fig. 2, EN_FWH and EN_LPC) that force the memory device to handle all future read and write operations by the selected protocol circuit (col. 7, ll. 43-45 and 46-58). Since the specification is clear that all future read and right operations will be handled by the selected protocol circuit (col. 7, ll. 43-58; Also please see col. 5, ll. 64-67 that states the memory device may be used in motherboards having chipsets employing either FWH *or* LPC). In other words the citation at col. 5, ll. 64-67 is teaching that there exists no such system that employs both FWH and LPC

simultaneously and as such the memory device (Fig. 2 and 9, 200 and 900) needs to select the appropriate protocol circuit only once.

Referring to figure 8 of Chang a circuit is shown for outputting the enable signals to the protocol circuits (easily modifiable by one of skill in the art to accomplish the single bit selection signal of figure 9). Let us say for example the memory device (Fig. 2 and 9, 200 and 900) is installed in a motherboard that employs the LPC communication protocol. According the specification a start code of '0000b' will be supplied to the memory device to initiate a transaction using the motherboard dependent LPC communication protocol. Also shown in the specification is a transaction enable signal LFrame (Fig. 5 and 6) that is active low and informs a device on the LPC communication bus that the transaction is beginning. Referring once again to figure 8, once the LPC communication bus supplies the '0000b' start code the NOR gate **802** outputs high signal to AND gate **806**. Concurrently with the supplying of the start code '0000b' the LFrame enable signal is also issued (active low) and inverted by the inverter **804** and supplied to the AND gate **806**. The AND gate **806** having been supplied with the two logic high signals outputs a logic high EN_LPC signal instructing the LPC protocol circuit to handle all future read and right operations (col. 7, ll. 43-45). When a read transaction like the one shown in figure 5, is initiated a start code and LFrame signal are supplied at time t1 thus causing the circuit of figure 8 to output a logic high EN_LPC signal. Next in times t2 through t8 the state of the LAD0-LAD3 lines (required to be '0000b' in order to output the EN_LPC signal) are constantly changing values and the LFrame logic low signal is raised to a logic high value. Therefore the EN_LPC signal would not be outputted to the LPC protocol circuit during the remainder of the transaction

and thus the memory device (Fig. 2 and 9, 200 and 900) would not be enabled to handle the remainder of the transaction. It is because of this fact the Examiner respectfully submits that there *must* be an inherent memory to hold and generate the value of EN_LPC at a logic high value because the specification of Chang supports the notion that the LPC protocol circuit (Fig. 2, 208) will be enabled to handle all future read and write operations (coil 7, ll. 43-45).

In summary the Examiner has shown that the invention of Chang inherently possess a user-selectable memory for storing a user selected protocol and generating the select signal according to the user selected protocol.

In regards to Goetting:

The Goetting reference was relied upon to show the obviousness of using an array non-volatile fuse memories. Contrary to applicant's position Goetting does disclose that the non-volatile fuse memory is capable of generating a select signal. Goetting discloses that non-volatile fuse memories are often used in conjunction with output cells such as multiplexers (i.e. the non-volatile fuse supplies the select signal). Goetting was then applied to Chang to teach the inherent user-selectable memories of Chang should be applied as non-volatile fuse memories that are programmed (fuses burned) once since the inherent memory must supply either an EN_LPC or EN_FWH to the appropriate protocol circuit such that all future read and write operations are handled by the appropriate protocol circuit. By instituting the non-volatile fuse memory of Goetting into Chang the EN_LPC or EN_FWH or SEL signal always supplies the appropriate value after initially receiving a proper start code value such that thereafter all read and write

operations are handled by the corresponding protocol circuit. Likewise by instituting the inherent memory as a non-volatile fuse memory, the value of the selection or enable signal is constant and never changes during failure events thus providing a reliable system.

In regards to Joo:

The Joo reference was relied upon to show that proving a mode selecting circuit responsive to a test signal for testing the memory device or for operating the memory device was beneficial because it allows the user to easily vary design margins and access times thus improving reliability and performance (Joo; col. 3, ll. 1-5). Applicant's arguments that Joo fails to teach a non-volatile that is user selectable and configured to store user selected protocol is moot because Joo was not relied upon to teach those aspects of the applicant's invention.

The prior art rejections from the Office Action dated June 22, 2005 will be re-provided below for applicant's convenience. For further clarification of the rejection of claim 1 applicant is invited to review the previously stated remarks with respect to the Chang and Goetting references.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US006851014B2) in view of Goetting (US 4783606).

All references below are made with respect to Chang except if otherwise noted.

For claim 1:

Chang teaches:

A memory device (Fig. 1, 108) for communicating with an integrated circuit (Fig. 1, 106) via a communication bus (Fig. 1, 120), said device comprising:

- an interface circuit for receiving communication signals from the communication bus, and for decoding the communication signals, and for generating a plurality of protocol signals and for outputting one of the plurality of protocol signals in response to a select signal (Fig. 9, items 204 and 210 [Operation Interface and Protocol Detection CKT] make up the interface circuit of applicant's invention; col. 8, ll. 25-49 teaches an embodiment of Chang that operates similar to the memory device of figure 2 except that the memory device of figure 9 uses a multiplexer instead of two enable signals, therefore references will be made to the memory device of figure 2 to explain the workings of devices not explicitly stated for the memory device of figure 9; col. 5, line 12 – col. 6, line 2) ;
- a non-volatile memory (Fig. 2, 202); and
- a controller for controlling the non-volatile memory; said controller responsive to said one protocol signal (Fig. 1, 106; col. 3, ll. 21-37).

With regards to a user selectable non-volatile memory for storing user selected protocol and for generating the select signal, corresponding to the user selected protocol the Examiner respectfully submits a memory is inherently present for storing the **SEL** signal of figure 9. Support for this assertion can be found in col. 7, ll. 43-46 (or ll. 56-58) and figure 7. The cited passage reads, "Thereafter, LPC/FWH protocol circuit 208/206 handles read and write operations for memory device in a well-known manner using the LPC/FWH communication protocol." By using *thereafter* it is implied the LPC or FWH protocol circuit will be enabled for the remainder of operation. This therefore implies a memory is used to supply the enable (or select) signal because if a memory was not used neither enable signals would be active. For this the Examiner directs the applicant's attention to figure 8 of Chang. Figure 8 teaches a programming logic circuit for receiving the user selected protocol and outputting selection signals to be an inherent memory which then sends the signals to the respective protocol circuits for enabling. If a memory was not present the signals indicative of an enabled protocol would activate/deactivate according to the value of the data or addresses that are inputs to the logic gates of figure 8 (NOR, inverter, & AND gates). Since none of the logic gates of figure 8 have memory the values at the inputs of the gates immediately affects the output. As such the enable signals would constantly toggle with values on the bus lines, thus enabling/disabling the protocol circuits. As applicant can clearly see, there must be an inherent memory to hold the appropriate enable signals for use with memory array 202 of figure 2. While a memory device of some type is inherently present, the disclosure of Chang does not expressly teach or suggest the use of a non-volatile memory for signaling an enable/selection signal.

Goetting teaches programmable logic devices that are typically created from an array of fuses (Goetting; col. 1, line 10). The programming logic device (PLD) is therefore non-volatile in that once a fuse is blown the PLD will maintain it's internal wiring state, thus providing a constant output (Goetting; col. 1, ll. 10-20). Often, PLDs are used in conjunction with output cells such as multiplexers like that of Chang figure 9.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the inherent memory of as a typical non-volatile PLD array of fuses such that the generated select signal would maintain its value in the event of power disruption thus providing reliable failure protection.

For claim 2:

The memory device of claim 1 wherein the interface circuit comprises:

- a decoding circuit for receiving the communication signals and for decoding the communication signals to generate a plurality of protocol signals (Fig. 2 and 9, 210; col. 5 line 44 – col. 6, line 2);
- a multiplexer for receiving the plurality of protocol signals and for generating one of the plurality of protocol signals in response to a select signal (Fig. 9, 902; col. 8, ll. 25-49).

For claim 3:

The memory device of claim 2 wherein the plurality of protocol signals represent protocol for LPC communication, FWH communication (various locations of the specification of Chang including col. 4, ll. 5-19).

For claim 4:

The memory device of claim 1 wherein the user selectable non-volatile memory comprises a non-volatile fuse (Goetting; col. 1, ll. 10-20).

For claim 5:

The memory device of claim 4 further comprising: a programming logic circuit for receiving the user selected protocol to program the non-volatile fuse (Fig. 8; col. 7, line 59 – col. 8, line 17).

For claim 6:

The memory device of claim 5 further comprising:

- said non-volatile fuse has an output (Goetting; col. 1, ll. 10-20);
- a fuse sense circuit for receiving the output and for generating a fuse control signal (a fuse sense circuit is an inherent feature of the PLD of Goetting. The sense circuit is needed to drive the logic value stored in the PLD. Support for this assertion is evidenced by Goetting et al. (5,039,885) (hereinafter Goetting2) Fig. 2, 31 [col. 3, ll. 47-50] which is incorporated by reference into the Goetting patent used above);
- a latch for receiving the fuse control circuit and for generating the select signal (Goetting incorporates by reference Goetting2, thus providing the entirety of the disclosure of

Goetting2 into the teaches of Goetting. As such Goetting2 teaches a PLD circuit can be enhanced by providing a latch to hold the output [col. 2, ll. 23-24].).

For claim 8:

A memory device for communicating with an integrated circuit via a communication bus, said device comprising:

- an interface circuit for receiving communication signals from the communication bus, and for decoding the communication signals, and for generating a plurality of protocol signals, and for outputting one of the plurality of protocol signals in response to a select signal (Fig. 9, items 204 and 210 [Operation Interface and Protocol Detection CKT] make up the interface circuit of applicant's invention; col. 8, ll. 25-49 teaches an embodiment of Chang that operates similar to the memory device of figure 2 except that the memory device of figure 9 uses a multiplexer instead of two enable signals, therefore references will be made to the memory device of figure 2 to explain the workings of devices not explicitly stated for the memory device of figure 9; col. 5, line 12 – col. 6, line 2);
- a non-volatile fuse for generating the select signal (As stated above, Chang implies the use of a memory for holding the value of the select signal of the multiplexer of figure 9 but does not expressly suggest the use of a non-volatile fuse memory. Goetting teaches programmable logic devices that are typically created from an array of fuses (Goetting; col. 1, line 10). The programming logic device (PLD) is therefore non-volatile in that once a fuse is blown the PLD will maintain it's internal wiring state, thus providing a

constant output (Goetting; col. 1, ll. 10-20). Often, PLDs are used in conjunction with output cells such as multiplexers like that of Chang figure 9.);

- a non-volatile memory (Fig. 2, 202);
- a controller for controlling the non-volatile memory; said controller responsive to said one protocol signal (Fig. 1, 106; col. 3, ll. 21-37); and
- a sensing circuit for detecting the communication signals and for programming the non-volatile fuse (a fuse sense circuit is an inherent feature of the PLD of Goetting. The sense circuit is needed to drive the logic value stored in the PLD. Support for this assertion is evidenced by Goetting et al. (5,039,885) (hereinafter Goetting2) Fig. 2, 31 [col. 3, ll. 47-50] which is incorporated by reference into the Goetting patent used above).

For claim 9:

The memory device of claim 8 wherein the interface circuit comprises:

- a decoding circuit for receiving the communication signals and for decoding the communication signals to generate a plurality of protocol signals (Fig. 2 and 9, 210; col. 5 line 44 – col. 6, line 2);
- a multiplexer for receiving the plurality of protocol signals and for generating one of the plurality of protocol signals in response to a select signal (Fig. 9, 902; col. 8, ll. 25-49).

For claim 10:

The memory device of claim 9 wherein the plurality of protocol signals represent protocol for LPC communication, FWI communication (various locations of the specification of Chang including col. 4, ll. 5-19).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US006851014B2) in view of Goetting (US 4783606) as applied to claim 6 above and further in view of Joo (US005596538A).

As discussed above, Chang in view of Goetting teach of a memory device with a common interface (Chang; Fig. 2 and 9, 204) with a protocol detection circuit (Chang; Fig. 2 and 9, 210) that selects a protocol based on decoded signals and applies the decoded signals as select signal (Chang; Fig. 9, SEL) which is outputted from a non-volatile fuse memory (Goetting; col. 1, ll. 10-20) to a multiplexer (Chang; Fig. 9, 902) as discussed above. Chang nor Goetting however teach a mode-selecting circuit responsive to a test signal for testing or operating the memory device.

Joo teaches a mode selecting circuit (Fig. 5, 30) that is responsive to a test signal (Fig. 5, 20) for testing the memory device (col. 3, ll. 7-33). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the mode selecting circuit of Joo into the memory device of Chang in view of Goetting such that based on accurate information regarding the semiconductor memory device as obtained by the vendor test, design margins and

an access time can be easily varied according to each semiconductor memory device, thereby improving a reliability and a performance.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

RMS